

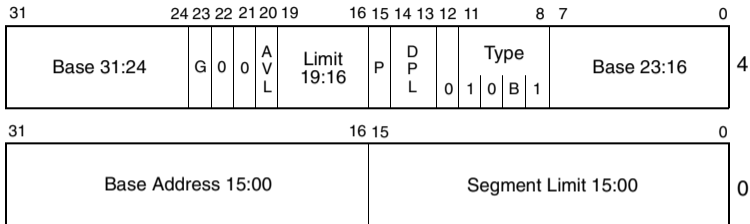
**Figure 6-1. Structure of a Task**

31	15	0	
I/O Map Base Address		T	100
		LDT Segment Selector	
		GS	96
		FS	92
		DS	88
		SS	84
		CS	80
		ES	76
		ES	72
EDI			68
ESI			64
EBP			60
ESP			56
EBX			52
EDX			48
ECX			44
EAX			40
EFLAGS			36
EIP			32
CR3 (PDBR)			28
		SS2	24
ESP2			20
		SS1	16
ESP1			12
		SS0	8
ESP0			4
		Previous Task Link	
			0

 Reserved bits. Set to 0.

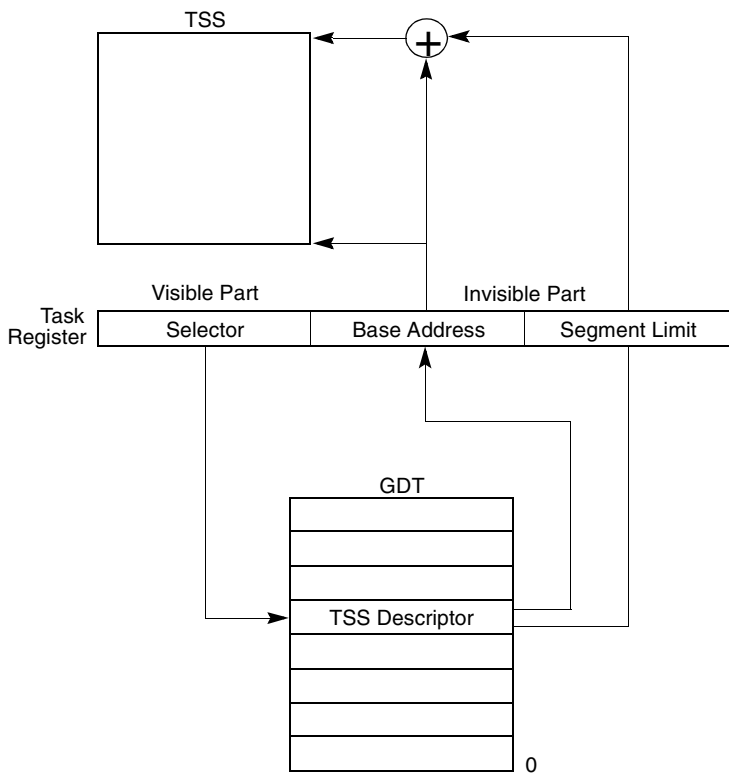
**Figure 6-2. 32-Bit Task-State Segment (TSS)**

## TSS Descriptor

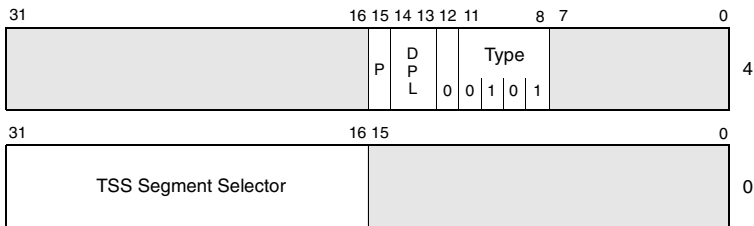


- AVL Available for use by system software
- B Busy flag
- BASE Segment Base Address
- DPL Descriptor Privilege Level
- G Granularity
- LIMIT Segment Limit
- P Segment Present
- TYPE Segment Type

**Figure 6-3. TSS Descriptor**



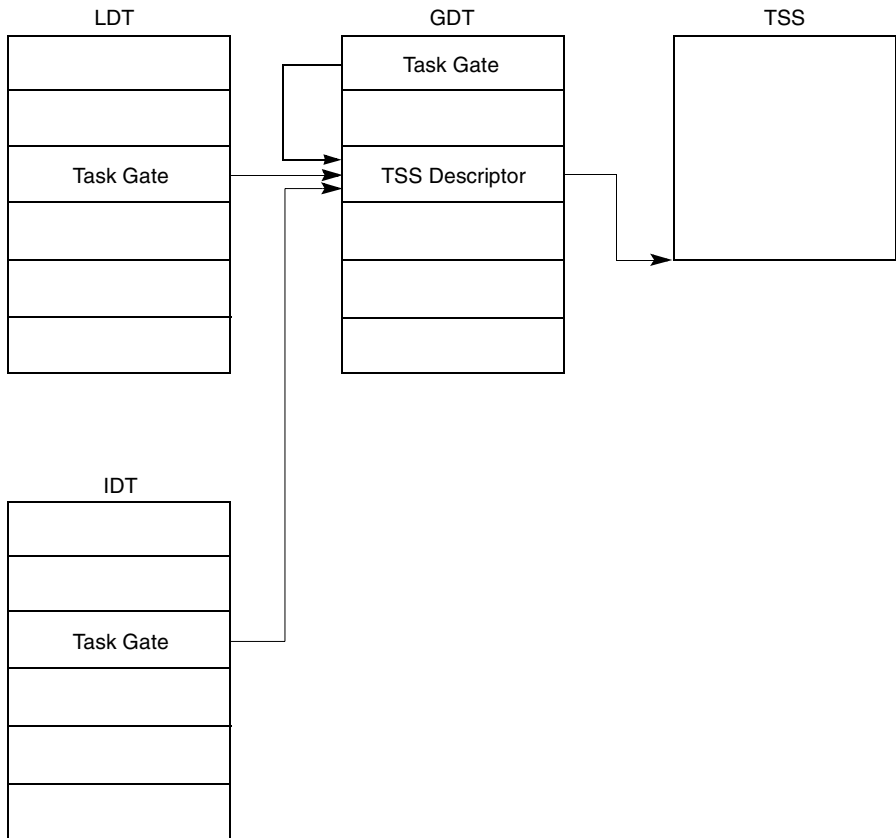
**Figure 6-4. Task Register**



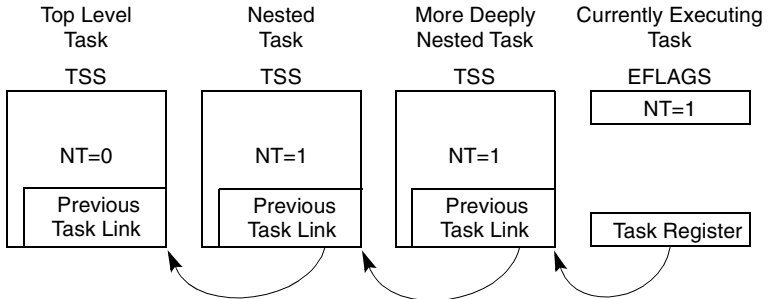
DPL Descriptor Privilege Level  
P Segment Present  
TYPE Segment Type

Reserved

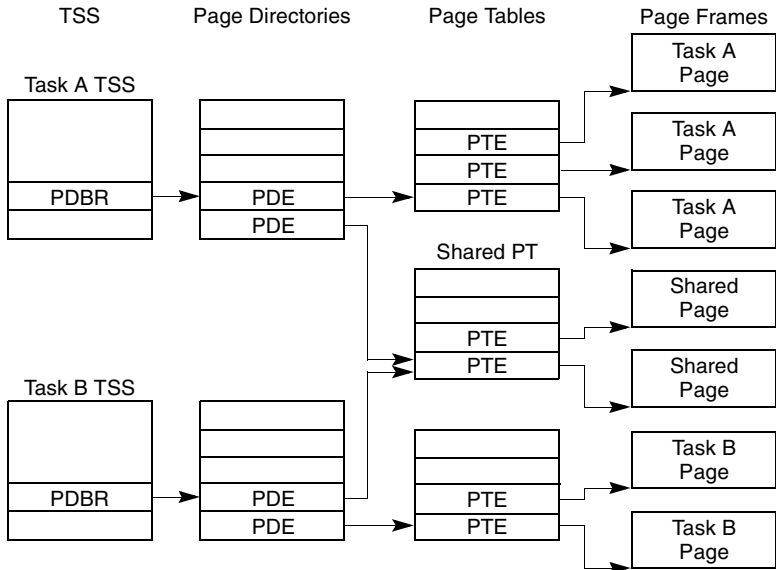
**Figure 6-5. Task-Gate Descriptor**



**Figure 6-6. Task Gates Referencing the Same Task**



**Figure 6-7. Nested Tasks**



**Figure 6-8. Overlapping Linear-to-Physical Mappings**