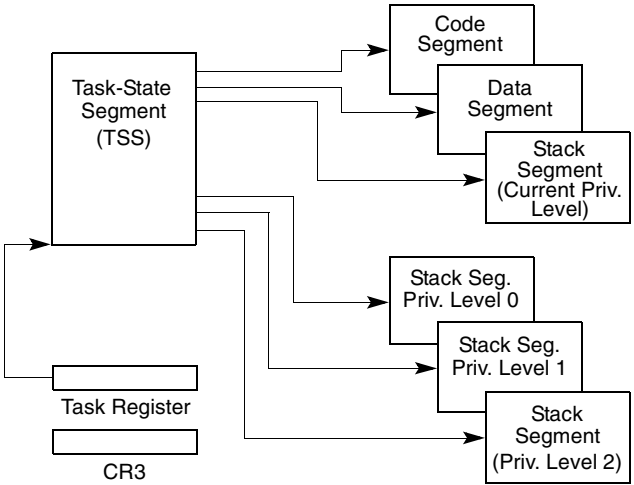


Figure 6-1. Structure of a Task

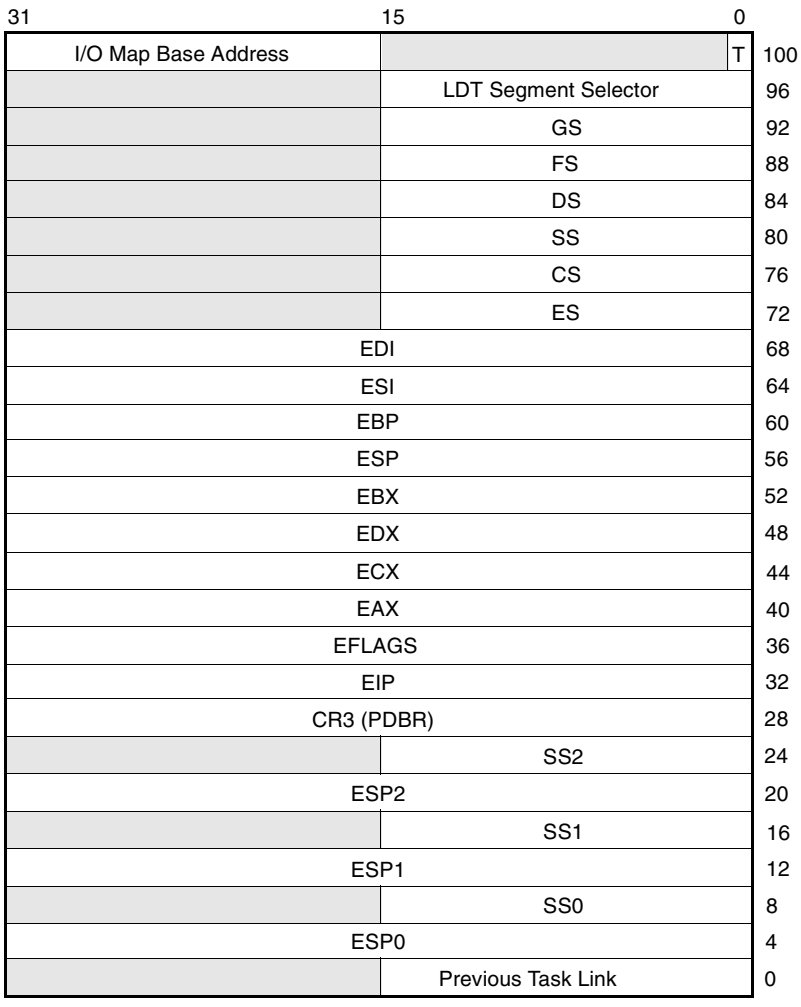
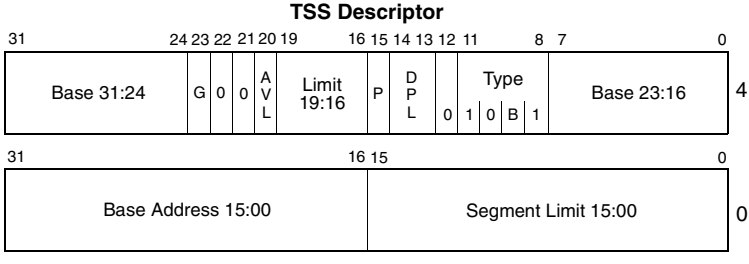


Figure 6-2. 32-Bit Task-State Segment (TSS)



AVL	Available for use by system software
B	Busy flag
BASE	Segment Base Address
DPL	Descriptor Privilege Level
G	Granularity
LIMIT	Segment Limit
P	Segment Present
TYPE	Segment Type

Figure 6-3. TSS Descriptor

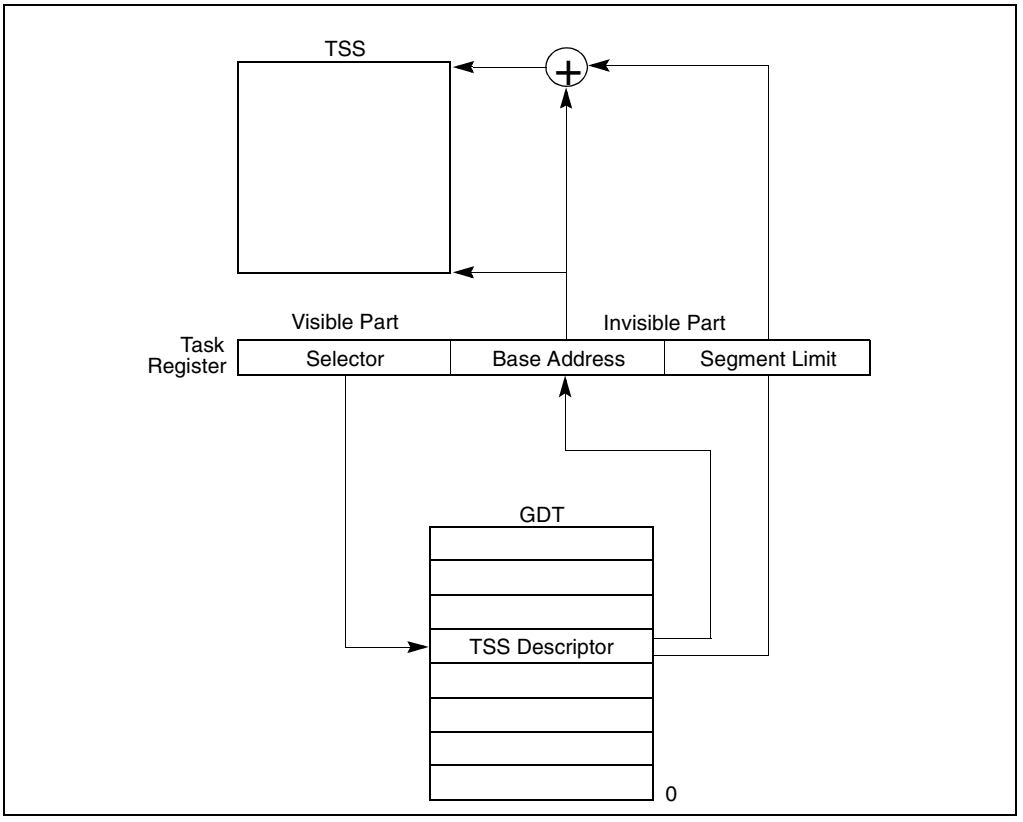


Figure 6-4. Task Register

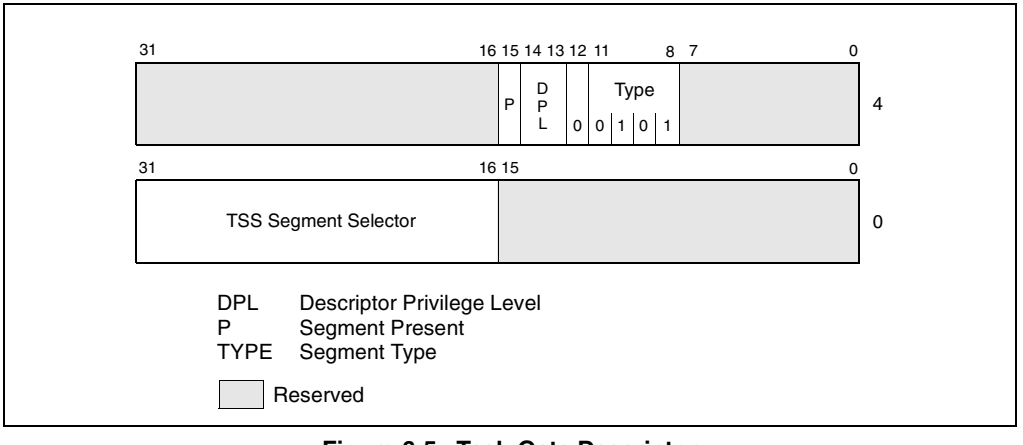


Figure 6-5. Task-Gate Descriptor

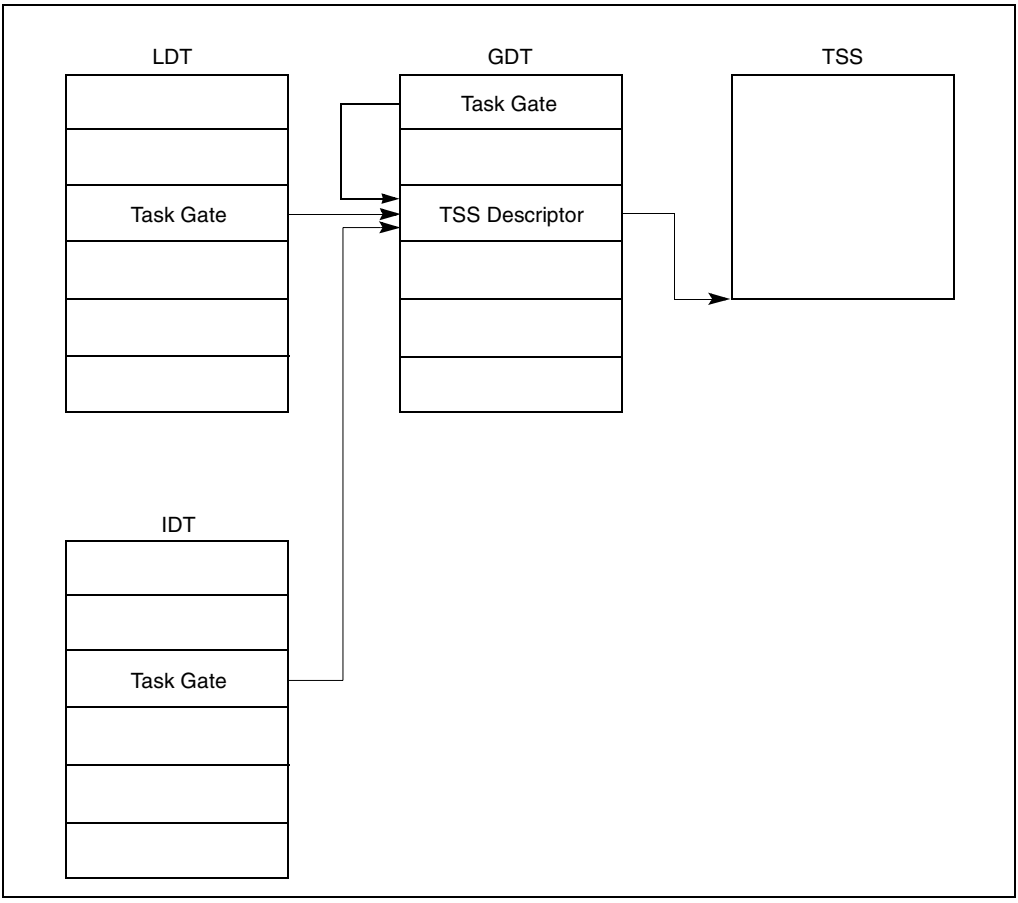


Figure 6-6. Task Gates Referencing the Same Task

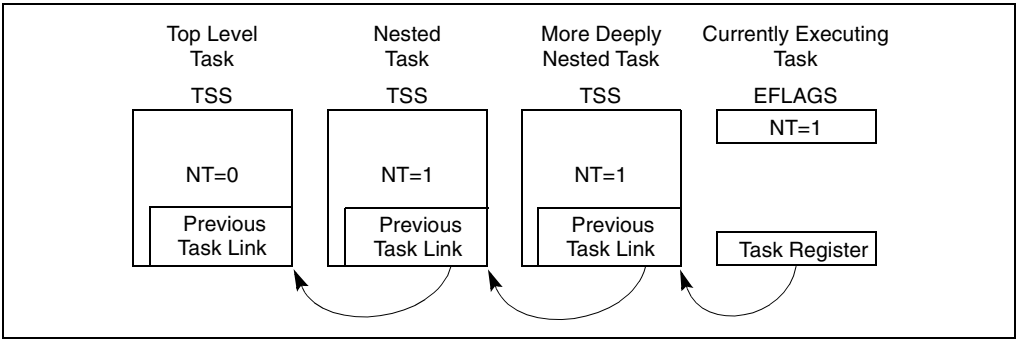


Figure 6-7. Nested Tasks

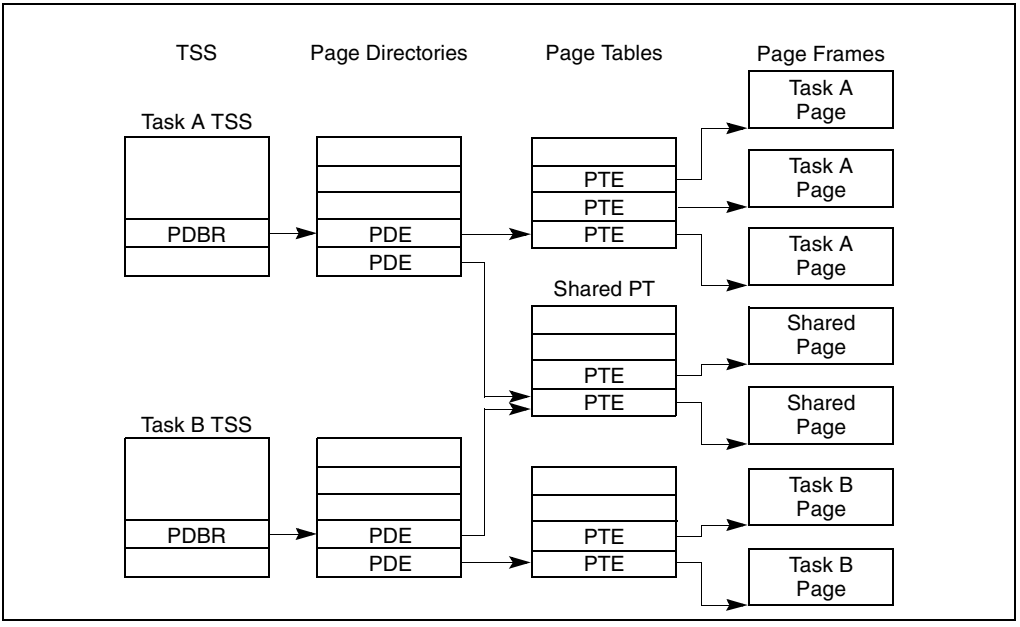


Figure 6-8. Overlapping Linear-to-Physical Mappings