

Figure 3-1. Segmentation and Paging



Figure 3-2. Flat Model



Figure 3-3. Protected Flat Model



Figure 3-4. Multi-Segment Model



Figure 3-5. Logical Address to Linear Address Translation



Figure 3-6. Segment Selector

Visible Part	Hidden Part	_
Segment Selector	Base Address, Limit, Access Information	CS
		SS
		DS
		ES
		FS
		GS

Figure 3-7. Segment Registers

31	24 23	22	21	20 1	9 16	15	14 13	12	11 8	7		0	
Base 31:24	G	D / B	0	A V L	Seg. Limit 19:16	Ρ	D P L	s	Туре		Base 23:16		4

31	16 15	0
Base Address 15:00	Segment Limit 15:00	(

- AVL Available for use by system software
- BASE Segment base address
- D/B Default operation size (0 = 16-bit segment; 1 = 32-bit segment)
- DPL Descriptor privilege level
- G Granularity
- LIMIT Segment Limit
- P Segment present
- S Descriptor type (0 = system; 1 = code or data)
- TYPE Segment type



Figure 3-9. Segment Descriptor When Segment-Present Flag Is Clear

Table 3-1. Code- and Data-Segment Types

	Туре	Field				
Decimal	11	10 E	9 W	8 A	Descriptor Type	Description
0	0	0	0	0	Data	Read-Only
1	0	0	0	1	Data	Read-Only, accessed
2	0	0	1	0	Data	Read/Write
3	0	0	1	1	Data	Read/Write, accessed
4	0	1	0	0	Data	Read-Only, expand-down
5	0	1	0	1	Data	Read-Only, expand-down, accessed
6	0	1	1	0	Data	Read/Write, expand-down
7	0	1	1	1	Data	Read/Write, expand-down, accessed
		С	R	Α		
8	1	0	0	0	Code	Execute-Only
9	1	0	0	1	Code	Execute-Only, accessed
10	1	0	1	0	Code	Execute/Read
11	1	0	1	1	Code	Execute/Read, accessed
12	1	1	0	0	Code	Execute-Only, conforming
13	1	1	0	1	Code	Execute-Only, conforming, accessed
14	1	1	1	0	Code	Execute/Read-Only, conforming
15	1	1	1	1	Code	Execute/Read-Only, conforming, accessed

Type Field Decimal Description Reserved 16-Bit TSS (Available) LDT 16-Bit TSS (Busy) 16-Bit Call Gate Task Gate 16-Bit Interrupt Gate 16-Bit Trap Gate Reserved 32-Bit TSS (Available) Reserved 32-Bit TSS (Busy) 32-Bit Call Gate Reserved 32-Bit Interrupt Gate 32-Bit Trap Gate

 Table 3-2.
 System-Segment and Gate-Descriptor Types



Figure 3-10. Global and Local Descriptor Tables



Figure 3-11. Pseudo-Descriptor Format

Table 3-3. Page Sizes and Physical Address Sizes

PG Flag, CR0	PAE Flag, CR4	PSE Flag, CR4	PS Flag, PDE	PSE-36 CPUID Feature Flag	Page Size	Physical Address Size
0	Х	Х	Х	х		Paging Disabled
1	0	0	Х	х	4 KBytes	32 Bits
1	0	1	0	х	4 KBytes	32 Bits
1	0	1	1	0	4 MBytes	32 Bits
1	0	1	1	1	4 MBytes	36 Bits
1	1	Х	0	х	4 KBytes	36 Bits
1	1	Х	1	х	2 MBytes	36 Bits



*32 bits aligned onto a 4-KByte boundary.

Figure 3-12. Linear Address Translation (4-KByte Pages)



Figure 3-13. Linear Address Translation (4-MByte Pages)

	Page-Directory Entry (4-K	Byt	e Pa	age	Т	ab	le))					
31		12	11	9	8	7	6	5	4	3	2	1	(
	Page-Table Base Address		Ava	ail	G	P S	0	А	P C D	P W T	U / S	R / W	F
	Available for system programmer's use Global page (Ignored) Page size (0 indicates 4 KBytes) Reserved (set to 0) Accessed Cache disabled Write-through User/Supervisor Read/Write Present												

Page-Table Entry (4-KByte Page)

31		12	11	9	8	7	6	5	4	3	2	1	0
	Page Base Address		Avai	I	G	P A T	D	А	P C D	P W T	U / S	R / W	Ρ
	Available for system programmer's use Global Page Page Table Attribute Index Dirty Accessed Cache Disabled Write-Through User/Supervisor Read/Write Present												

Figure 3-14. Format of Page-Directory and Page-Table Entries for 4-KByte Pages and 32-Bit Physical Addresses

Page-Directory Entry (4-MByte Page)

31	22	21 13	12	11 9	8	7	6	5	4	3	2	1	0
	Page Base Address	Reserved	P A T	Avail.	G	PS	D	A	PCD	P W T	U/ S	R∕ ∀	Ρ
	Page Table Attribute Available for system Global page Page size (1 indicate Dirty Accessed Cache disabled Write-through User/Supervisor Read/Write Present	Index programmer's use - es 4 MBytes)											

Figure 3-15. Format of Page-Directory Entries for 4-MByte Pages and 32-Bit Addresses











Figure 3-18. Linear Address Translation With PAE Enabled (4-KByte Pages)



Figure 3-19. Linear Address Translation With PAE Enabled (2-MByte Pages)

63						36	35		32	
Reserved (set to 0)										
31	12	11	1	9	8 5	4	3	2 1	0	
	Page-Directory Base Address	A	vail		Reserved	P C D	P W T	Res.	Ρ	

Page-Directory Entry (4-KByte Page Table)

63								36	35	;		32
Reserved (set to 0)										Ba Ad	se dr.	
21		10.11	0	0	7	6	5	1	2	0	1	0

Page-Table Base Address Avail 0 0 0 A P P U R D T S W V<	31	121	11 9	8	1	6	Э	4	3	2		U
	Page-Table Base Address		Avail	0	0	0	A	P C D	P W T	U / S	R / W	Ρ

Page-Table Entry (4-KByte Page)

63					-					36	35			32
	Reserved (set to 0)													
31		1	2	11	9	8	7	6	5	4	3	2	1	0
	Page Base Address			Ava	il	G	P A T	D	A	P C D	P W T	U/S	R / W	Р

Figure 3-20. Format of Page-Directory-Pointer-Table, Page-Directory, and Page-Table Entries for 4-KByte Pages with PAE Enabled

Page-Directory-Pointer-Table Entry

63					-	36	35	5	32
Reserved (set to 0)									ə r.
31	12	: 11	1	9	8 5	4	3	2 1	0
	Page Directory Base Address	,	Avail		Reserved	P C D	P W T	Res	. P

Page-Directory Entry (2-MByte Page)

63										36	35	6		32
Reserved (set to 0)														
31 21	20	13	12	11	9	8	7	6	5	4	3	2	1	0
Page Base Address	Reserved (set to	0)	P A T	Avai		G	1	D	A	P C D	P W T	U / S	R / W	Ρ

Figure 3-21. Format of Page-Directory-Pointer-Table and Page-Directory Entries for 2-MByte Pages with PAE Enabled



Figure 3-22. Linear Address Translation (4-MByte Pages)

Figure 3-23 shows the format for the page-directory entries when 4-MByte pages and 36-bit physical addresses are being used. Section 3.7.6., "Page-Directory and Page-Table Entries" describes the functions of the flags and fields in bits 0 through 11.



Figure 3-23. Format of Page-Directory Entries for 4-MByte Pages and 36-Bit Physical Addresses



Figure 3-24. Memory Management Convention That Assigns a Page Table to Each Segment