

Figure 2-1. IA-32 System-Level Registers and Data Structures

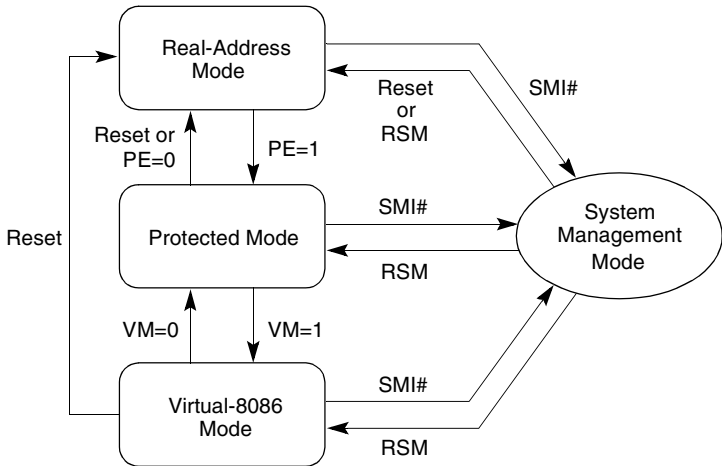


Figure 2-2. Transitions Among the Processor's Operating Modes

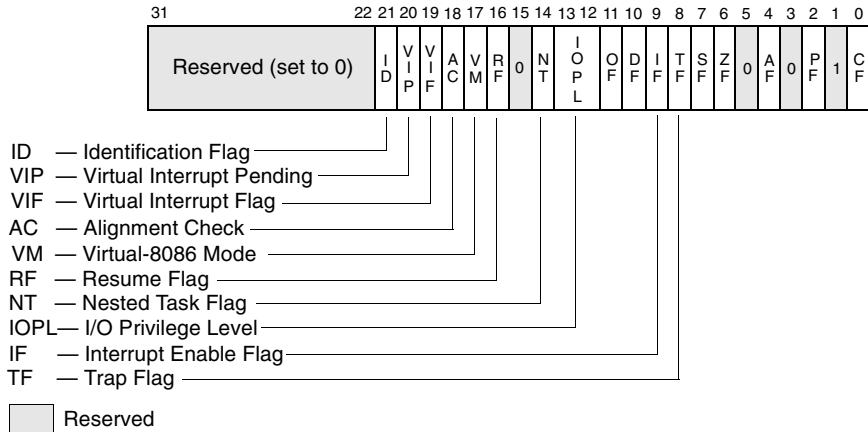


Figure 2-3. System Flags in the EFLAGS Register

System Table Registers

	47		16	15		0
GDTR	32-bit Linear Base Address			16-Bit Table Limit		
IDTR	32-bit Linear Base Address			16-Bit Table Limit		

System Segment Registers

Segment Descriptor Registers (Automatically Loaded)

	15		0			Attributes
Task Register	Seg. Sel.	32-bit Linear Base Address		Segment Limit		
LDTR	Seg. Sel.	32-bit Linear Base Address		Segment Limit		

Figure 2-4. Memory Management Registers

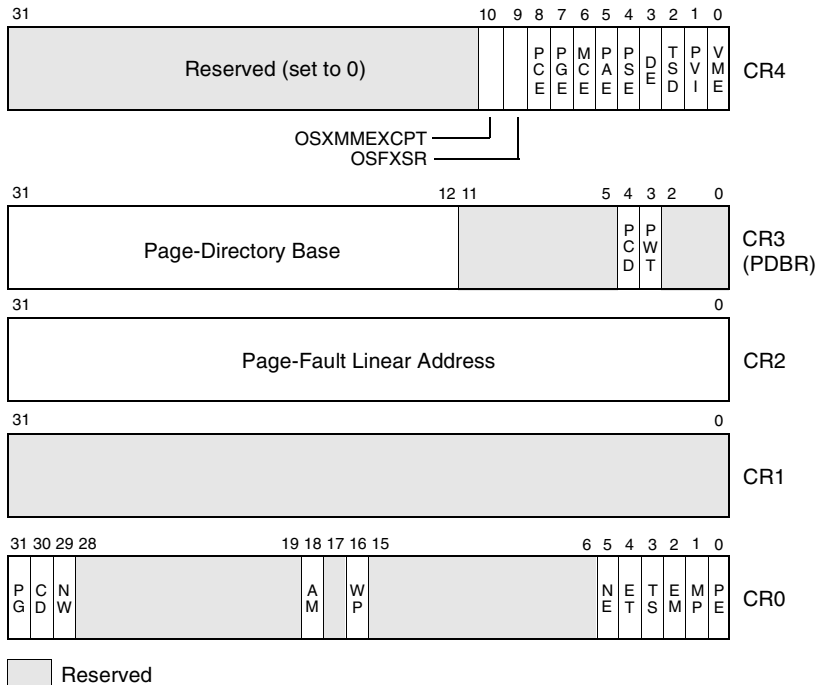


Figure 2-5. Control Registers