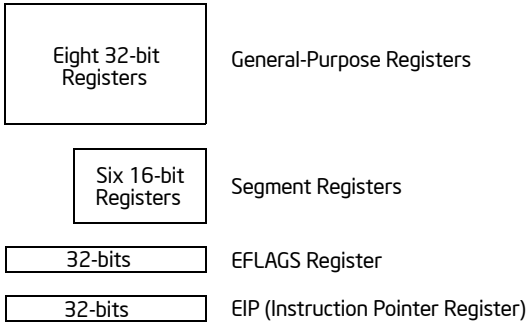
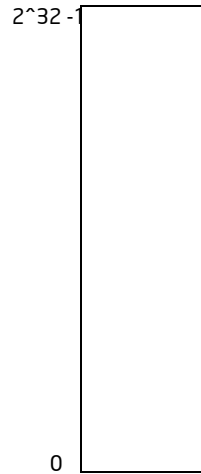


Basic Program Execution Registers

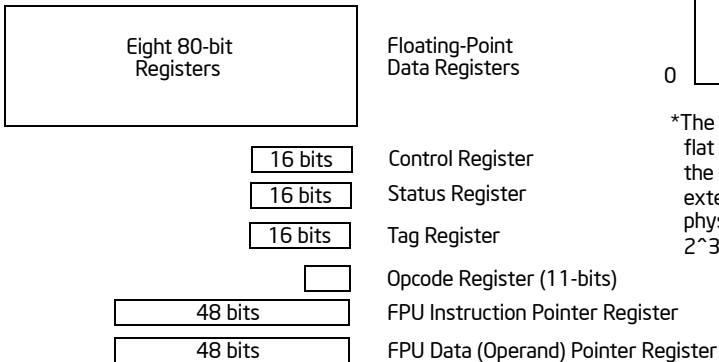


Address Space*

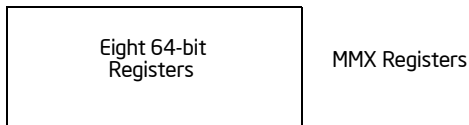


*The address space can be flat or segmented. Using the physical address extension mechanism, a physical address space of $2^{36} - 1$ can be addressed.

FPU Registers



MMX Registers



XMM Registers

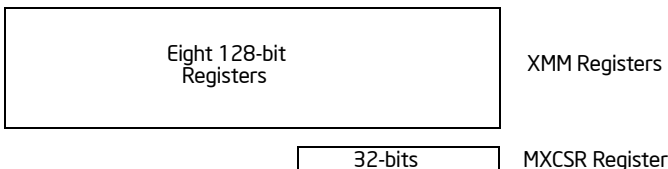
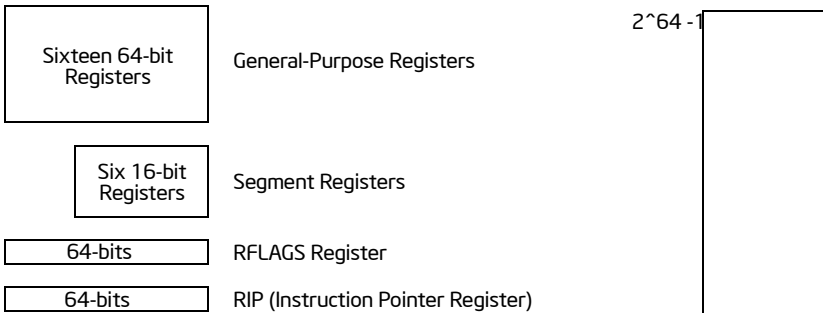


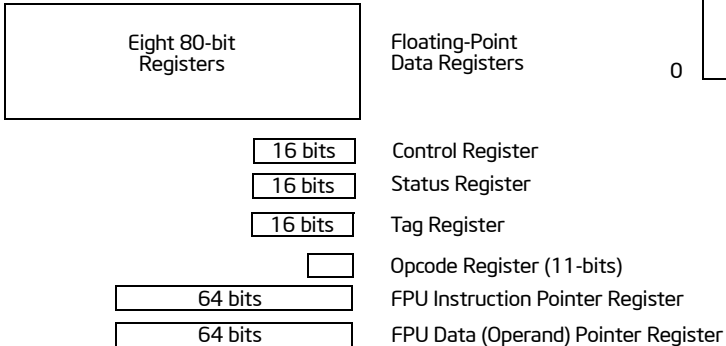
Figure 3-1. IA-32 Basic Execution Environment for Non-64-bit Modes

Basic Program Execution Registers

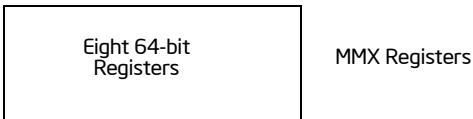
Address Space



FPU Registers



MMX Registers



XMM Registers

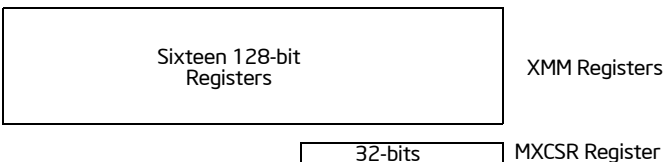


Figure 3-2. 64-Bit Mode Execution Environment

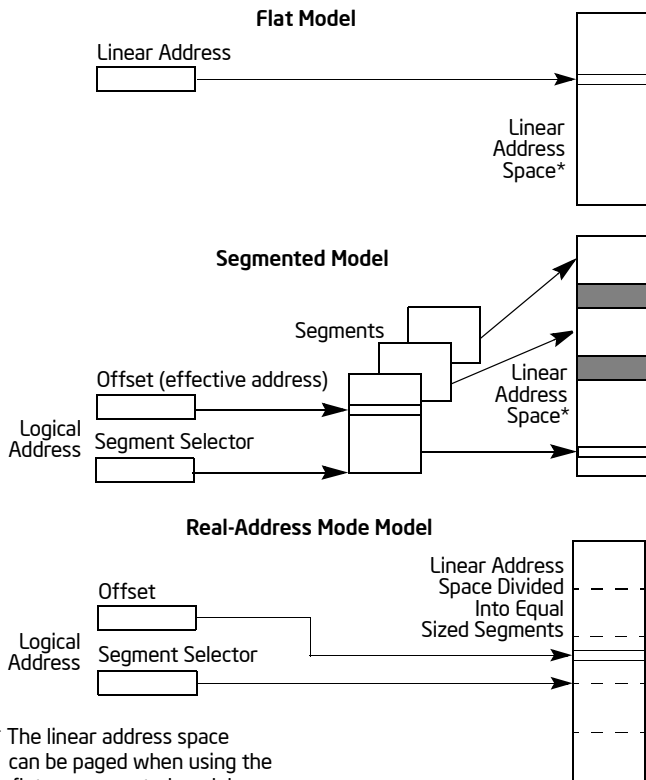


Figure 3-3. Three Memory Management Models

Table 3-1. Instruction Pointer Sizes

	Bits 63:32	Bits 31:16	Bits 15:0
16-bit instruction pointer	Not Modified		IP
32-bit instruction pointer	Zero Extension	EIP	
64-bit instruction pointer	RIP		

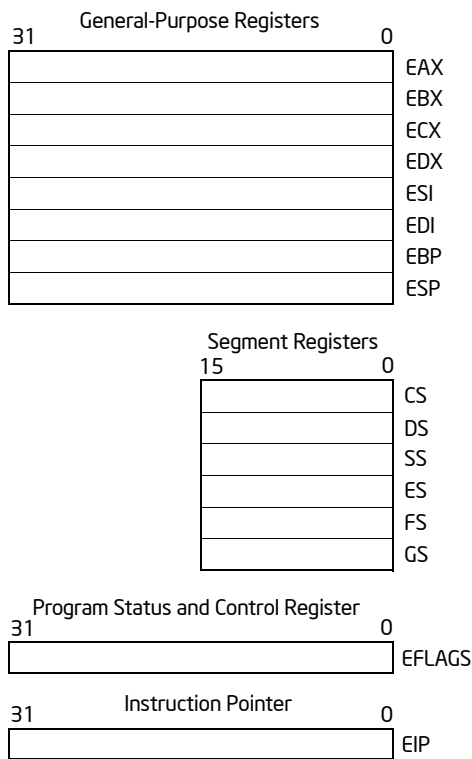


Figure 3-4. General System and Application Programming Registers

General-Purpose Registers

31	16	15	8	7	0	16-bit	32-bit
	AH		AL			AX	EAX
	BH		BL			BX	EBX
	CH		CL			CX	ECX
	DH		DL			DX	EDX
	BP						EBP
	SI						ESI
	DI						EDI
	SP						ESP

Figure 3-5. Alternate General-Purpose Register Names

Table 3-2. Addressable General Purpose Registers

Register Type	Without REX	With REX
Byte Registers	AL, BL, CL, DL, AH, BH, CH, DH	AL, BL, CL, DL, DIL, SIL, BPL, SPL, R8L - R15L
Word Registers	AX, BX, CX, DX, DI, SI, BP, SP	AX, BX, CX, DX, DI, SI, BP, SP, R8W - R15W
Doubleword Registers	EAX, EBX, ECX, EDX, EDI, ESI, EBP, ESP	EAX, EBX, ECX, EDX, EDI, ESI, EBP, ESP, R8D - R15D
Quadword Registers	N.A.	RAX, RBX, RCX, RDX, RDI, RSI, RBP, RSP, R8 - R15


Segment Registers



CS
DS
SS
ES
FS
GS

The segment selector in each segment register points to an overlapping segment in the linear address space.

Linear Address Space for Program



Overlapping Segments
of up to
4 GBytes
Beginning at
Address 0

Figure 3-6. Use of Segment Registers for Flat Memory Model

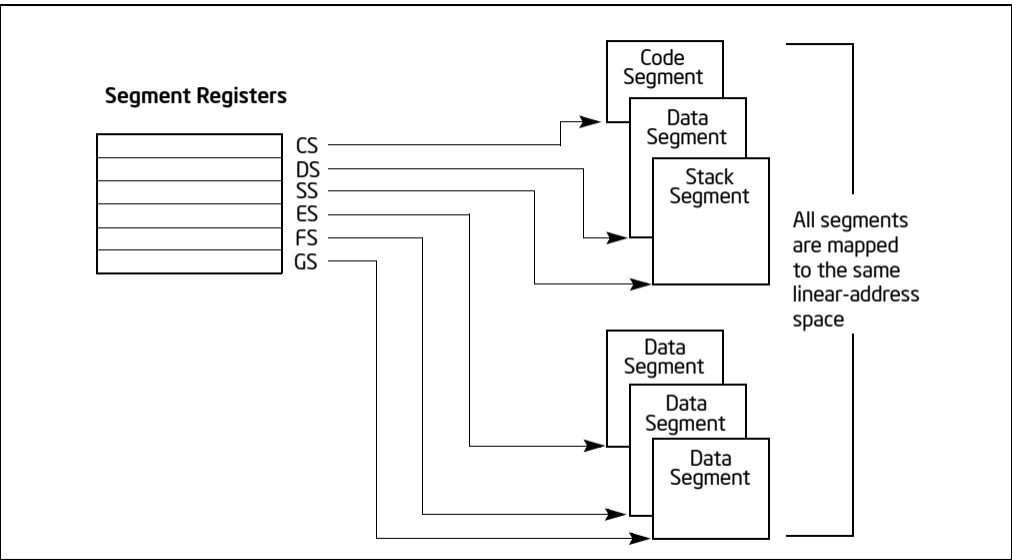
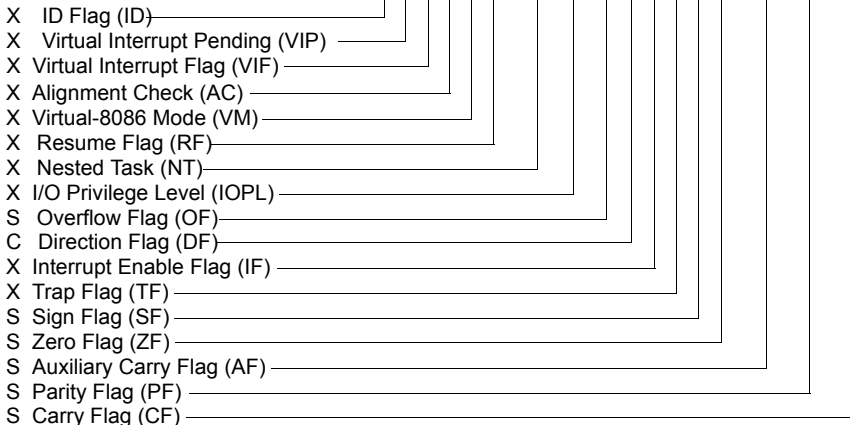
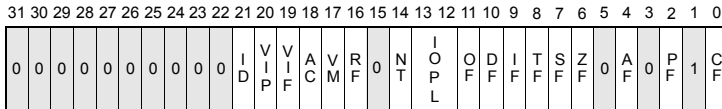


Figure 3-7. Use of Segment Registers in Segmented Memory Model



- S Indicates a Status Flag
- C Indicates a Control Flag
- X Indicates a System Flag

Reserved bit positions. DO NOT USE.
Always set to values previously read.

Figure 3-8. EFLAGS Register

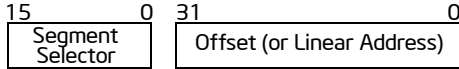


Figure 3-9. Memory Operand Address

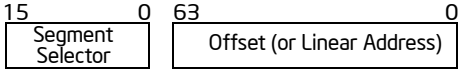
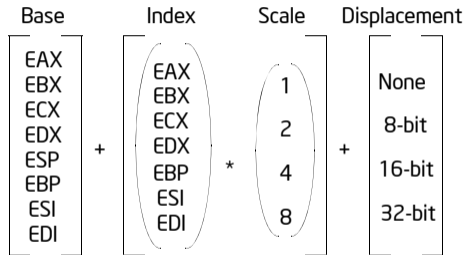


Figure 3-10. Memory Operand Address in 64-Bit Mode



$$\text{Offset} = \text{Base} + (\text{Index} * \text{Scale}) + \text{Displacement}$$

Figure 3-11. Offset (or Effective Address) Computation