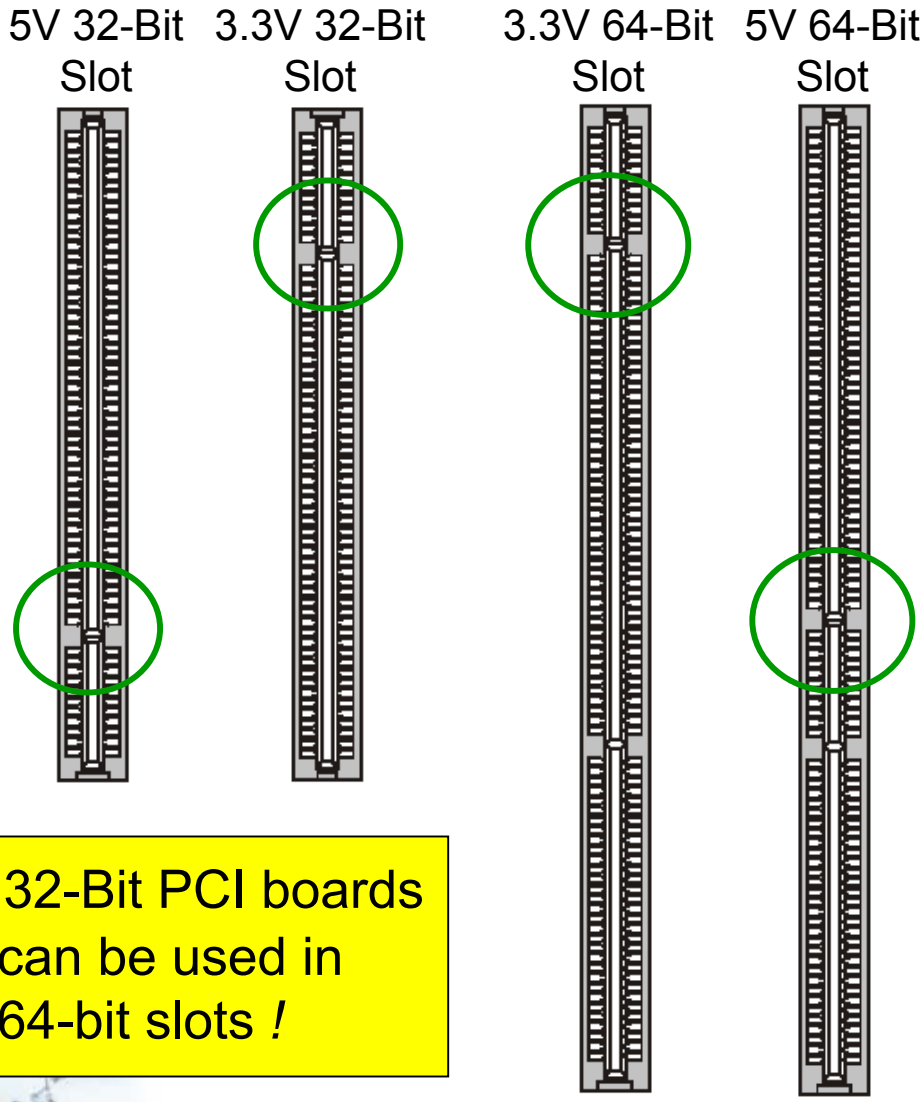
PCI Technology

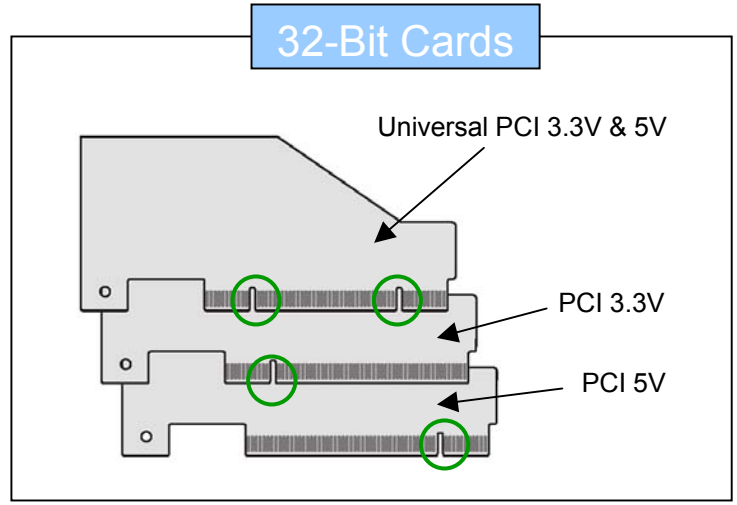
- Conventional PCI
  - Initial PCI 1.0 proposal by Intel in 1991
  - Introduced by PCI-SIG as PCI 2.0 in 1993
  - Version 2.1 approved in 1995
  - Recent version 2.3 approved in March 2002
- PCI-X
  - Version 1.0 approved in September 1999
  - Version 2.0 approved in July 2002
- PCI Express
  - Formerly known as 3GIO
  - Version 1.0 approved in July 2002

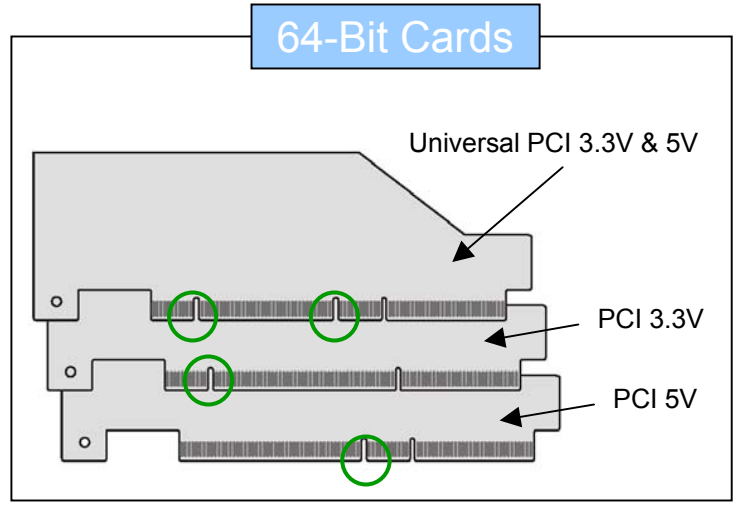
Conventional PCI

- Plug-and-Play Functionality
- Standard PCI is 32 bit and operates at 33 MHz
  - Throughput 133 MB/sec
- PCI 2.1 introduced
  - Universal PCI cards supporting both 3.3V and 5V
  - 64 Bit slots and 66 MHz capability
    - 32-Bit throughput @ 66 MHz: 266 MB/sec
    - 64-Bit throughput @ 66 MHz: 532 MB/sec
- PCI 2.3 system no longer supports 5V-only adapters
  - 3.3V and Universal PCI products are still fully supported *!*

32-Bit vs 64-Bit Slots/Boards







- 32-Bit PCI boards can be used in 64-bit slots *!*

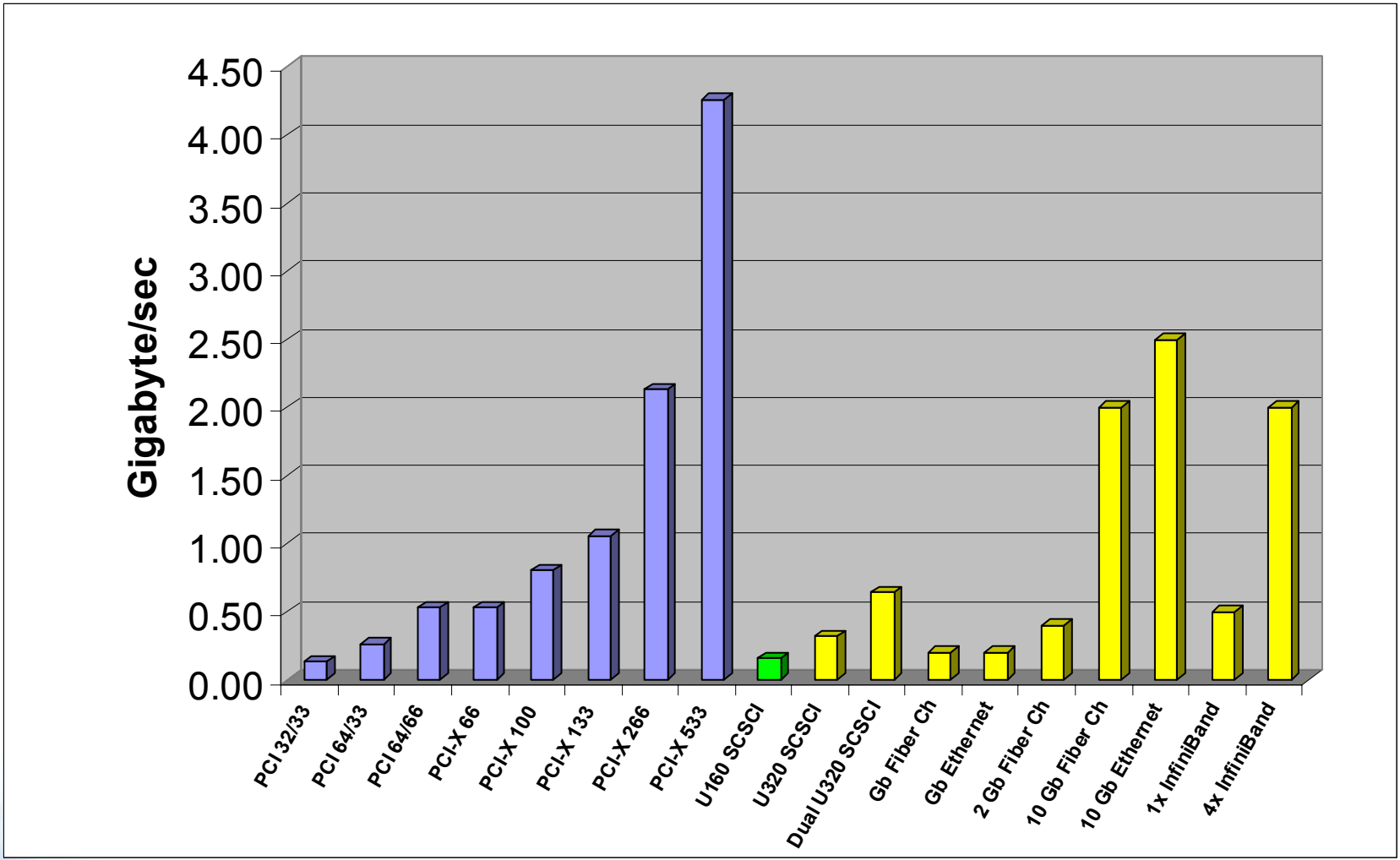
PCI-X 1.0

- Based on existing PCI architecture
- 64-Bit slots with support for 3.3V and Universal PCI
  - No support for 5V-only boards *!*
- Fully backwards-compatible
  - Conventional 33/66 MHz PCI adapters can be used in PCI-X slots
  - PCI-X adapters can be used in conventional PCI slots
- Provides two speed grades: 66 MHz and 133 MHz
  - The *slowest board* dictates the maximum speed on a particular bus *!*
- Targeted at high-end data networking and storage network applications

PCI-X 2.0

- Based on PCI-X 1.0
  - Still fully backwards-compatible
- Introduces ECC (Error Correction Codes) mechanism to improve robustness and data integrity
- Provides two additional speed grades
  - PCI-X 266: 266 MHz (2.13 GB/sec)
  - PCI-X 533: 533 MHz (4.26 GB/sec)
- Bandwidth sufficient to support new breed of cutting-edge technologies
  - 10 Gigabit Ethernet / Fiber Channel
  - 4X / 12X InfiniBand

PCI / PCI-X Performance vs Demand

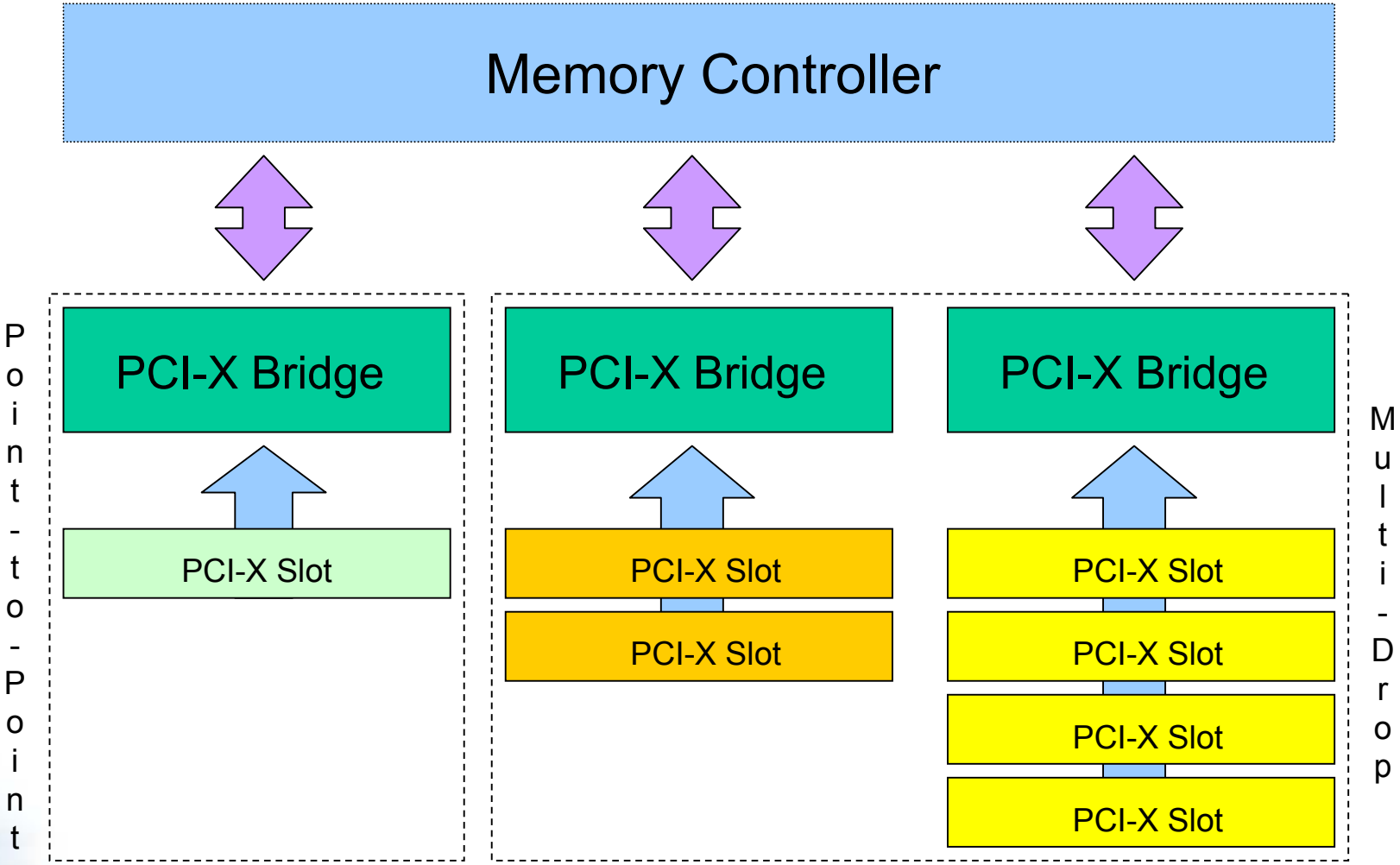


Source: PCI-SIG

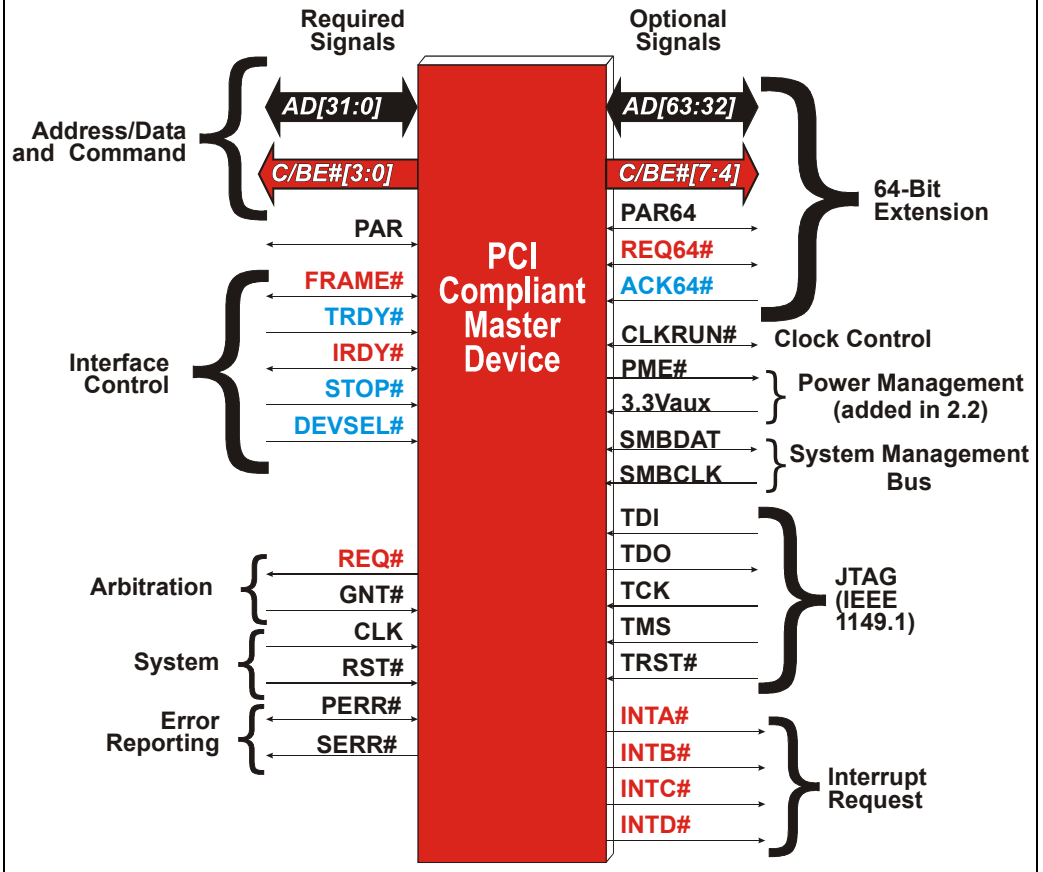
PCI-X Speed Limitations

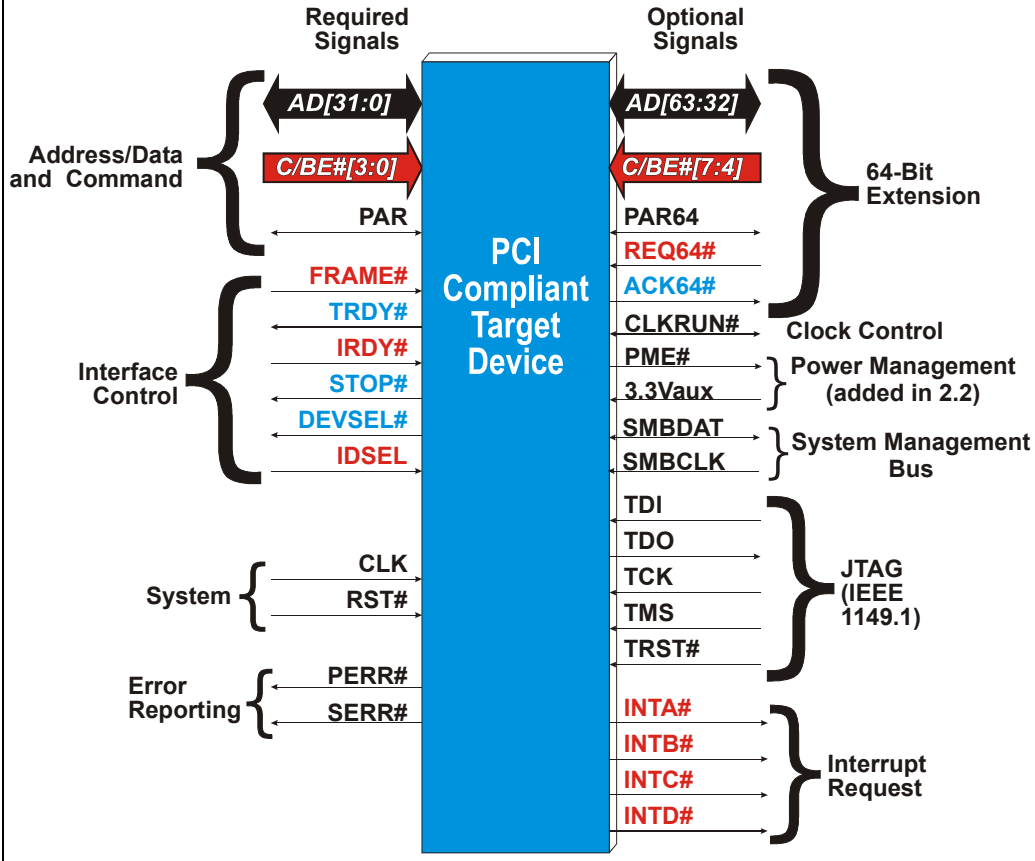
- PCI-X supports point-to-point and multi-drop loads
- Highest speed grades are supported *exclusively* with point-to-point loads
  - PCI-X 133
  - PCI-X 266
  - PCI-X 533
- Two PCI-X 133 loads operate at 100 MHz
- Four loads operate at a maximum of 66 MHz
- OEMs can build connector-less systems with multiple loads utilizing high speed grades

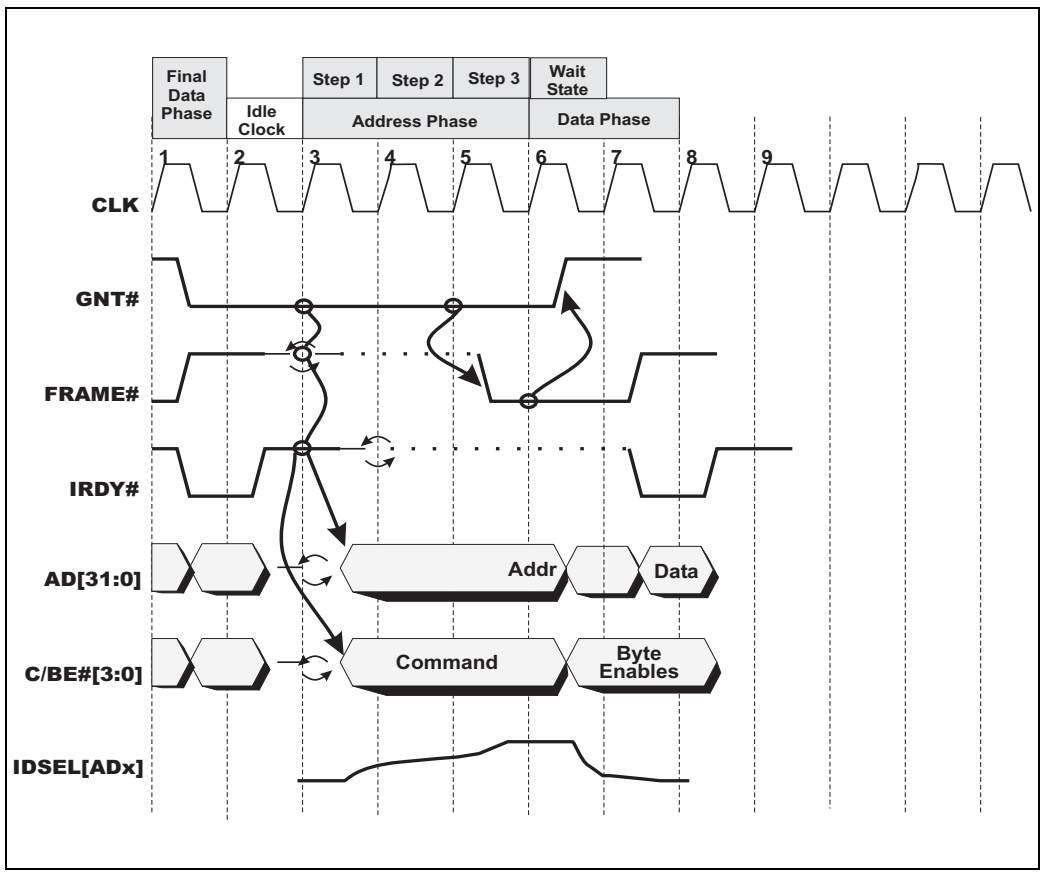
PCI-X Speed Limitations



- Maximum speed 133 / 266 / 533 MHz
- Maximum speed 100 MHz
- Maximum speed 66 MHz


Required Signals
Optional Signals
Address/Data and Command
AD[31:0]
C/BE#[3:0]
AD[63:32]
C/BE#[7:4]
64-Bit Extension
PAR
PAR64
REQ64#
ACK64#
PCI Compliant Master Device
Interface Control
FRAME#
TRDY#
IRDY#
STOP#
DEVSEL#
CLKRUN#
Clock Control
PME#
3.3Vaux
Power Management (added in 2.2)
SMBDAT
SMBCLK
System Management Bus
TDI
TDO
TCK
TMS
TRST#
JTAG (IEEE 1149.1)
Arbitration
REQ#
GNT#
System
CLK
RST#
Error Reporting
PERR#
SERR#
INTA#
INTB#
INTC#
INTD#
Interrupt Request


Required Signals
Optional Signals
PCI Compliant Target Device
Address/Data and Command
AD[31:0]
C/BE#[3:0]
PAR
AD[63:32]
C/BE#[7:4]
PAR64
REQ64#
ACK64#
64-Bit Extension
Interface Control
FRAME#
TRDY#
IRDY#
STOP#
DEVSEL#
IDSEL
CLKRUN#
Clock Control
PME#
3.3Vaux
Power Management (added in 2.2)
SMBDAT
SMBCLK
System Management Bus
TDI
TDO
TCK
TMS
TRST#
JTAG (IEEE 1149.1)
System
CLK
RST#
Error Reporting
PERR#
SERR#
INTA#
INTB#
INTC#
INTD#
Interrupt Request


Final Data Phase
Idle Clock
Step 1
Step 2
Step 3
Wait State
Address Phase
Data Phase
1
2
3
4
5
6
7
8
9
CLK
GNT#
FRAME#
IRDY#
AD[31:0]
Addr
Data
C/BE#[3:0]
Command
Byte Enables
IDSEL[ADx]